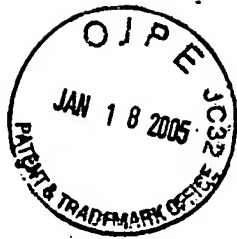


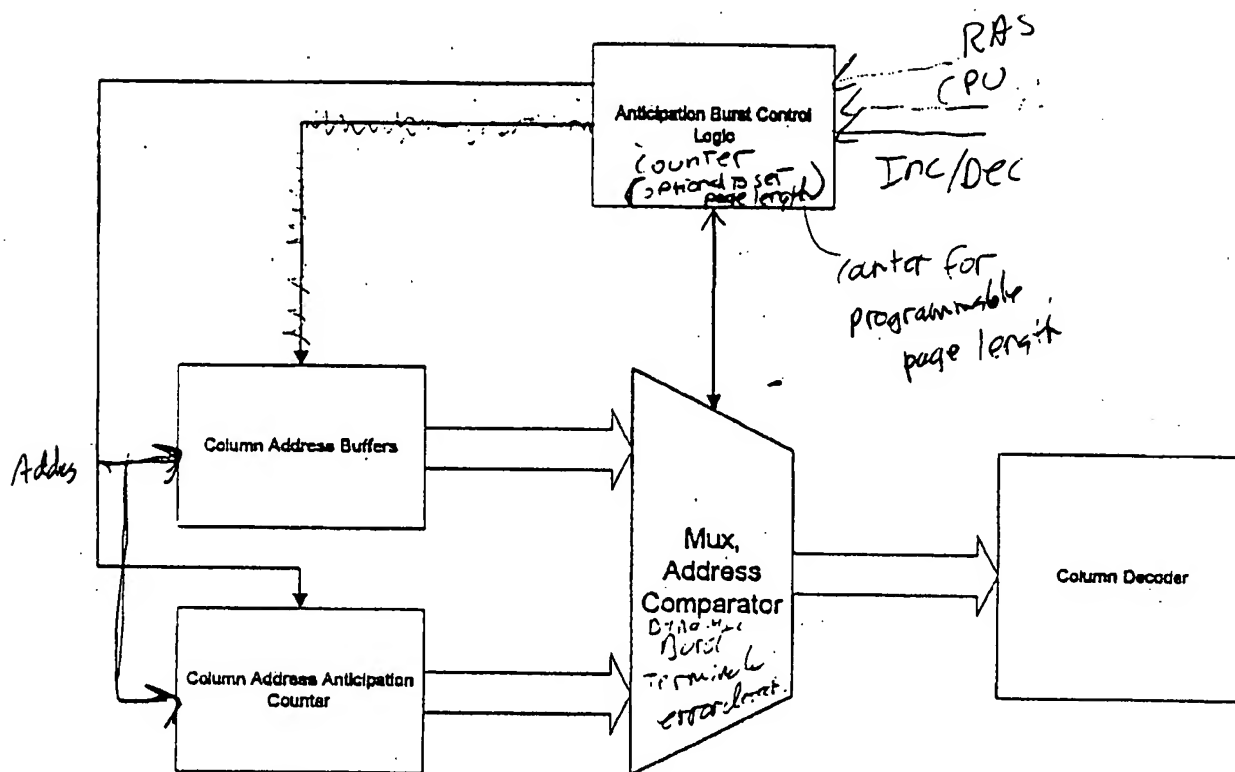
Fig. 3



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P.3

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Memory System Speed Enhancement  
Block Diagram

Erik Erlandson, David Tremblay

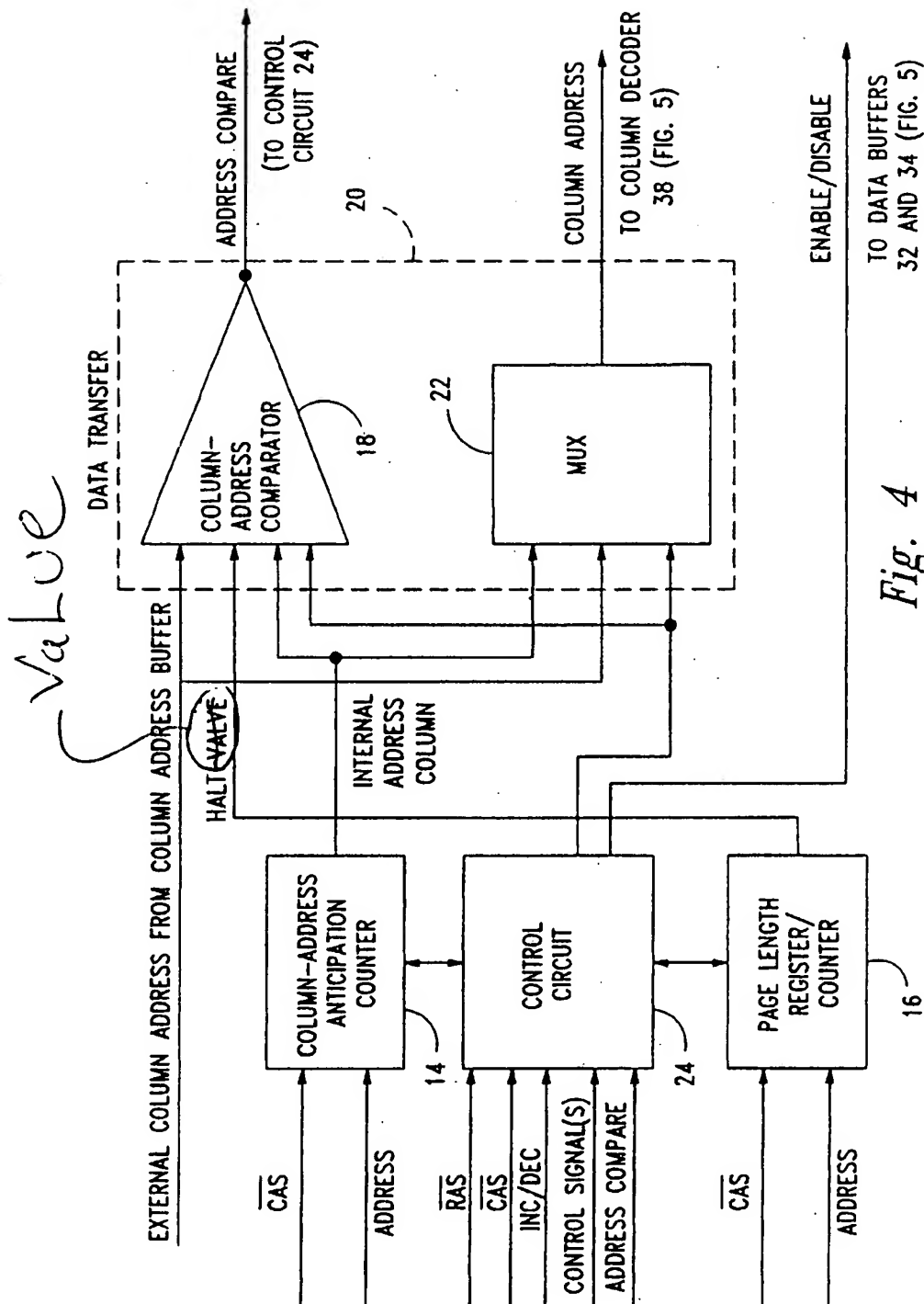


Fig. 4